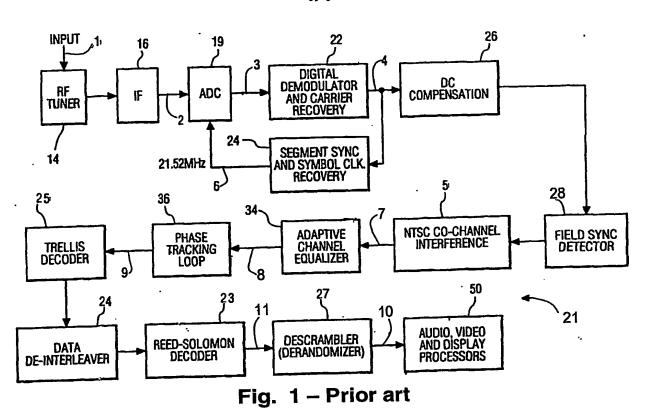
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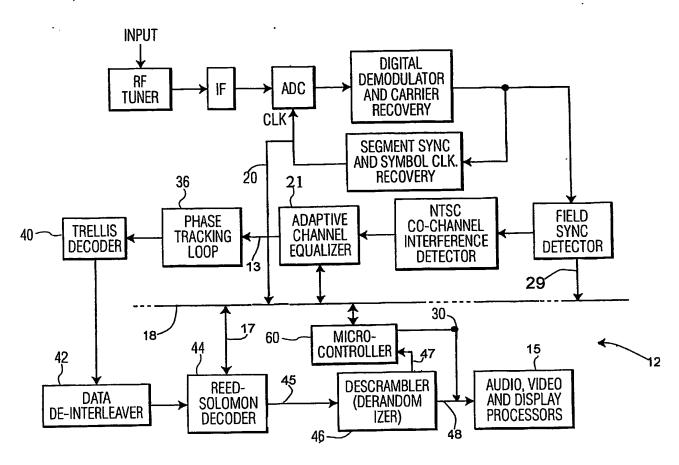


Fig. 2 - System

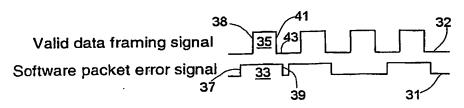


Fig. 3 - Waveforms

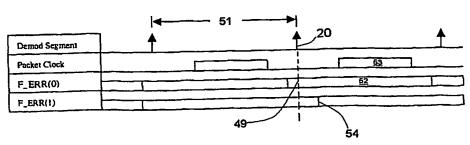


Fig. 4 – Timing

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bclr	2. int stat1	039	ora	#1
	ms_timer_count	040	bra	apply_gate
	_	041	lda	PCNTL
	ms_timer_count	042	and	#0xFE
	#0x6D	043	sta	i_temp0
	CAP_RAM_TRIG	044		sw_ferr_cnt+1
	#0x2D	045		#1
sta	CAP_RAM_TRIG			sw_ferr_cnt+1
lda	CAP_RAM_BASE			sw_ferr_cnt
and	#0x80			#0
ldx	ng_prt_in			sw_ferr_cnt
sta	next_gate, x			i_temp0
txa	_			PCNTL
eor	#1		txa	
sta	ng_ptr_in			#1
inc	pkt_cnt			ng_ptr_out
lda	pkt_cnt			field_flag
cmp	#170			no_field
bne	enb_wait		_	sync_cnt
lda	#1			
sta	ferr_dly			sync_cnt
jmp	chk_field	-		#55
lda	ferr_dly			no_field
nop				field_flag
deca				#15
bne	ferr_delay_idle			ferr_dly
lda	ferr_mod			pkt_cnt
inca				ferr_mod
cmp	#3			ng_ptr_in
bne	store_ferr_mod			ng_ptr_out
inc	ferr_dly			d int state
clra				1, int_stat1
sta				field_flag
ldx		-		ng_ptr_out
lda				#1
ora				ng_ptr_out
bne	gate_on			sync_cnt
lda	PCNTL	0/6	πs	
	Ida and Idx sta txa eor sta inc Ida cmp bne Ida sta jmp Ida nop deca bne Ida inca cmp bne inc clra sta Idx Ida ora bne	Ida ms_timer_count inca sta ms_timer_count Ida #0x6D sta CAP_RAM_TRIG Ida #0x2D sta CAP_RAM_BASE and #0x80 Idx ng_prt_in sta next_gate, x txa eor #1 sta ng_ptr_in inc pkt_cnt Ida pkt_cnt cmp #170 bne enb_wait Ida #1 sta ferr_dly jmp chk_field Ida ferr_dly nop deca bne ferr_delay_idle Ida ferr_mod inca cmp #3 bne store_ferr_mod inc ferr_dly clra sta ferr_mod Ida next_gate, x ora ferr_enable bne gate_on	Ida	Ida ms_timer_count 040 bra inca 041 Ida sta ms_timer_count 042 and Ida #0x6D 043 sta sta CAP_RAM_TRIG 044 Ida Ida #0x2D 045 add sta CAP_RAM_TRIG 046 sta Ida CAP_RAM_BASE 047 Ida and #0x80 048 adc Idx ng_ptr_in 049 sta sta ng_ptr_in 049 sta sta ng_ptr_in 053 eor inc pkt_cnt 053 eor inc pkt_cnt 054 sta Ida pkt_cnt 055 Idx cmp #170 056 beq bne enb_wait 057 Ida ida ferr_dly 061 onca jmp chk_field 060 cmp

Fig. 5 – Listing

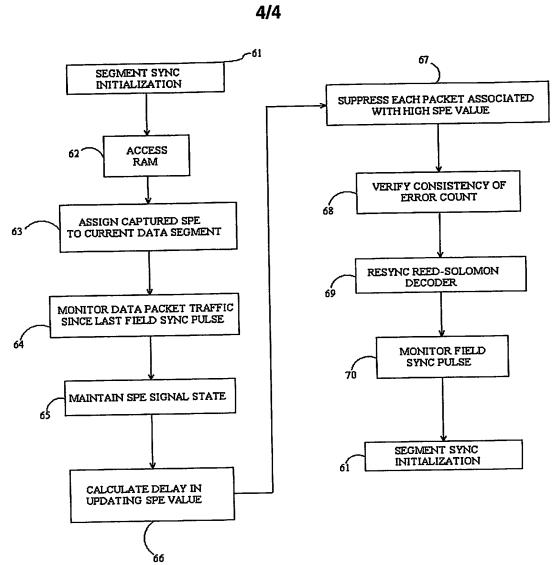


Fig. 6 - Flowchart